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#14 Appeal Brief
9-26-03

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Grace Alicea

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of: BULLIS, et al.

Date: September 16, 2003

Serial No: 09/409,940

Group Art Unit: 2123

Filed: September 30, 1999

Examiner: Ferris III, F.

For: METHOD AND SYSTEM FOR PROVIDING HIERARCHICAL SELF-CHECKING IN ASIC SIMULATION

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF COVER LETTER

Sir:

Submitted herewith are an original and two copies of Appellant's Brief on Appeal which is submitted under 37 C.F.R. 1.192 in connection with the above-identified Patent Application. The Brief includes and Appendix.

Please charge the Appeal Brief filing fee of $320.00 to Deposit Account Number 50-0563 (IBM Corporation). A duplicate copy of this paper is attached.

Very truly yours,

SAWYER LAW GROUP LLP

September 16, 2003

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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APPELLANT'S BRIEF

Attorney for Appellants
International Business Machines Corp.
Sawyer Law Group LLP

TOPICAL INDEX

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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APPELLANT'S BRIEF ON APPEAL

Sir:

Appellant herein files an Appeal Brief drafted in accordance with the provisions of 37 C.F.R. § 1.192(c) as follows:

I. REAL PARTY IN INTEREST

Appellant respectfully submits that the above-captioned application is assigned, in its entirety to International Business Machines Corp. of Armonk, New York.

II. RELATED APPEALS AND INTERFERENCES

Appellant states that, upon information and belief, he is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 are pending. Application Serial No. 09/409,940 (the instant application) as originally filed included claims 1-23. In an Amendment dated December 4, 2002, claims 1, 10, and 17 were amended. Claim 1 was amended to recite that the snooper monitors the interface of the island under test, that the checker determines the desired output based upon the input and that the generator includes intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator, the request requesting that the generator perform a particular simulation on the island. Similarly, claims 17 and 20 were amended to recite that the interface of the island under test is monitored, that the desired output of the island under test is determined based upon an input to the island, and that the input is provided to the island using a generator including intelligence to provide the input to the island based only upon data and a request provided by the test case(s) that the generator perform a particular simulation on the island. The specification was also amended to further clarify the operation of the method and system in accordance with the present invention. In particular, Figures 7A-7C were added. A declaration (First Declaration) under 37 C.F.R. 1.132 was also provided. In response to the Final Office Action, the Response dated May 20, 2003 provided remarks and a second declaration (Second Declaration) under 37 C.F.R. 1.132. Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 are on appeal and all applied prospective rejections concerning claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 are herein being appealed.

IV. STATUS OF AMENDMENT

There is no pending Amendment to the claims and the Second Declaration has not been objected to.

V. SUMMARY OF THE INVENTION

The present invention provides a method and system for simulating an integrated circuit during development of the integrated circuit. The integrated circuit has an island that includes an interface. The method and system include a snooper, a checker and a generator. The snooper is coupled with an interface, monitors the interface, and obtains an output provided by the island during simulation. Specification, page 12, lines 8-13. The checker is coupled with the interface and determines the desired output based upon the input(s) to the island and checking the output to determine whether the output is the desired output. Specification, page 12, lines 17-19. The generator is coupled with the interface and provides an input to the interface during simulation. Specification, page 12, lines 20-21. The generator is coupled with a test case that directs the generator. More specifically, the generator includes intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator. Specification, page 13, lines 2-4. The request requests that the generator perform a particular simulation on the island. Using the method and system in accordance with the present invention, more exhaustive testing can be done using fewer, simpler test cases. Specification, page 13, lines 4-5. Moreover, the snooper, checker, and generator can communicate with other snoopers, checkers, and generators. Specification, page 13, lines 5-9. In addition, the snooper and checker can remain coupled with the interface. Specification, page 13, lines 10-16. Consequently, step-wise checking of the islands in the integrated circuit can be achieved. Specification, page 16, lines 13-14. In

addition, the snoopers, checkers, and generators may be reused, thereby conserving resources. Specification, page 19, lines 3-4. Thus, the snoopers, checkers, and generators are general in nature and need only be developed once for a particular integrated circuit. Specification, page 19, lines 4-6.

For example, Figure 4A depicts embodiments of the snooper, checker, and generator coupled with various interfaces of an island. Figure 4B depicts the embodiments of the snooper, checker, and generator coupled with various islands to provide step-wise, or hierarchical, checking of the islands in the device being tested. The snoopers, checkers, and generators are used in conjunction with simplified test cases (not shown in Figures 4A and 4B). This is in contrast to the conventional mechanism for testing islands, which utilizes conventional test cases and models, such as those depicted in Figure 2B.

VI. ISSUES

The issues presented are:

(1) whether claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 are each unpatentable under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains; and

(2) 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 are each unpatentable under 35 U.S.C. § 103 as being obvious in light of U.S. Patent No. 6,182,258 (Hollander) in view of U.S. Patent No. 6,006,024 (Guruswamy).

VII. GROUPING OF CLAIMS

Appellant hereby states that claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 do not stand or fall together, but rather claims 1, 2, 3, 4, 5, 6, 7, 8, and 9 are one group, claims 10, 11, 12, 13, 14, 15, and 16 are another group, and claims 17, 18, 19, 20, 21, 22, and 23 are a third group. Therefore, claims 1-9, 10-16, and 17-23 constitute three (3) separate groups.

VIII. ARGUMENTS

A. Summary of the Applied Rejections

In the Final Office Action, dated February 20, 2003, the Examiner rejected claims 1-23 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains. With respect to claim 1, the Examiner cited the use of the terms "snooper," "interface," "checker," and "generator." The Examiner indicated that the specification "does not disclose an algorithm or technique for the implementation of either the 'snooper' or 'the interface.'" The Examiner also indicated that the recited interface is not disclosed in the specification and that "[w]hile numerous industry standard electronic interfaces . . . do exist, the applicants have not identified a standard interface nor have they disclosed their own design." With respect to the checker, the Examiner indicated that it is not disclosed how the checker performs the claimed checking. Similarly, with respect to the generator, the Examiner stated that "no description of the interface coupling or the related inputs and outputs is provided. Further, no description or explanation of how the generator is 'directed by a test case' is given and there is no description of how the generator actually functions." The Examiner had similar rejections to independent claims 10 and 17.

The Examiner further rejected claims 1-23 under 35 U.S.C. §.103 as being unpatentable over Hollander in view of Guruswamy. In particular, the Examiner cited Hollander as teaching the recited system, method, and computer code for verifying an integrated circuit design that monitors (snoops) the simulation of the integrated circuit, using a checker, a test generator, and a test case. The Examiner indicated that Hollander does not explicitly teach verification of a substrate incorporating cells via an island. Consequently, the Examiner cited Guruswamy as teaching a cell layout generation system environment that includes islands for an integrated circuit.

Appellant also notes that in the Final Office Action, the Examiner objected to the First Declaration. In response, Appellant submitted the Second Declaration to which the Examiner has not objected.

Appellant respectfully requests that the Board reverse the Examiner's final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 under 35 U.S.C. § 112, first paragraph, and the Examiner's final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 under 35 U.S.C. § 103.

B. The Cited Prior Art

Appellant agrees that Hollander describes a modular system that dynamically tests integrated circuits. The modular system of Hollander includes a test generation module and a checking module. Hollander, col. 4, line 66-col. 5, line 25. The system of Hollander is dynamic, which means that the test vectors can be generated in concurrence with the device being tested and can be controlled by feedback of the device. Hollander, col. 3, lines 10-13. The test generation module automatically creates inputs. Hollander col. 4, line 66-col. 5, line 7. The checking module dynamically checks the performance of the integrated circuit based upon these inputs. Hollander

does state that this dynamic checking can include synchronizing the checking module with the test generation module. Hollander, col. 5, lines 18-25 and col. 8, lines 29-32. The performance of the integrated circuit is thus verified. However, Appellant has found no indication in the cited portion of Hollander that the synchronizing or other portions of the dynamic checking includes using the checking module to generate the desired outputs based upon the inputs from the test generation module.

The cited portions of Guruswamy describe a method and system for laying out components of an integrated circuit. Guruswamy, Abstract. The cited portions of Guruswamy also describe islands as portions of the integrated circuit having at least a particular size. Guruswamy, col. 50, lines 29-30. The size and shape of the islands are then "grown" by laying out additional islands. Guruswamy, col. 50, lines 47-66. However, Appellant has found no mention in the cited portions of Guruswamy of checking the behavior of the integrated circuit being laid out. More particularly, Appellant has found no mention in the cited portions of Guruswamy of using a checker to not only check the outputs of the island under test, but also to generate the desired outputs based upon the inputs.

C. Claims 1-23 Are Not Unpatentable Under 35 U.S.C. § 112, First Paragraph.

Appellant respectfully submits that the applied rejections of claims 1-23 under 35 U.S.C. § 112, first paragraph, are without merit as the Examiner has completely failed to explain why the specification fails to describe, in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims.

Independent claims 1, 10, and 17 recite a system, method, and computer-readable medium used in providing simulation for an integrated circuit having an island. The island in the integrated circuit includes an interface. Independent claim 1 recites the use of a snooper to monitor the interface and obtain an output from the island. Claim 1 also recites that the checker generates a desired output and check the output obtained by the snooper against this desired output. In addition, claim 1 recites the use of a generator that provides the input to the island in response to a request from a test case to perform a particular simulation on the island and data provided by the test case. Similarly, independent claims 10 and 17 recite the steps of and instructions for monitoring the interface of the island to obtain an output, determining a desired output based upon the input and checking this output against the desired output, and providing the input to the island. Claims 10 and 17 further recite that the input is provided to the island using a generator including intelligence to provide the input to the island based only upon data and a request provided by the at least one test case that the generator perform a particular simulation on the island.

In the Final Office Action, the Examiner rejected claims 1-23 under 35 U.S.C. § 112, first paragraph, based upon the use of the terms interface, snooper, checker, and generator. The Examiner also indicated that how the generator is directed by the test case is not sufficiently disclosed in the specification.

Appellant respectfully disagrees with the Examiner. In particular, Appellant respectfully submits that one of ordinary skill in the art is one who has worked in the field of simulating the behavior of and testing the performance of integrated circuits. Appellant also respectfully submits that one of ordinary skill in the art would also be at least peripherally involved in using and/or developing the conventional test cases and conventional models described in the specification, page

2, line 14-page 7, line 10 and Figures 1-2D. In particular, one of ordinary skill in the art would have utilized the conventional test cases and models to test the behavior of islands. For these and the reasons described below, Appellant respectfully submits that one of ordinary skill in the art would understand the terms interface, snooper, checker, generator, and how the test case directs the generator. Appellant respectfully submits that these terms are described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims

Appellant respectfully submits that the term "interface" is described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims. In particular, one of ordinary skill in the art would readily understand that the term interface includes conventional input/output (I/O) ports and the accompanying processes for a circuit being simulated on a test bench. Signals are input to or output from the representation of the integrated via the interface. Specification, page 2, lines 2-5 and page 7, lines 2-5. In addition, as discussed above and in the BACKGROUND OF THE INVENTION, the interfaces are already present in the integrated circuits of the prior art. Specification, page 2, lines 1-5. Thus, one of ordinary skill in the art would have known of coupling the conventional models and conventional test cases to the interfaces of islands. One such conventional system and method are depicted in Figure 2B and described in the specification, page 2, lines 18-22 and page 3, lines 2-5. Therefore, as indicated in the Second Declaration, one of ordinary skill in the art would recognize the interfaces of the island typically include I/O ports for connecting to the island and a process for controlling the I/O ports that operates in a system-clock domain where simulation time is advanced. Such I/O ports, as well as the processes that control the I/O ports, may depend upon the specific integrated circuit being

tested. Consequently, although a particular type of interface for a particular integrated circuit is not described in the specification, Appellant respectfully submits that one of ordinary skill in the art, particularly one who has tested integrated circuits using conventional means, would understand the term "interface." More particularly, Appellant respectfully submits that one of ordinary skill in the art would readily understand that such an interface includes an I/O port for a circuit being checked on a test bench and a process for controlling the I/O ports in a system-clock domain where simulation time is advanced, thereby allowing behavior of the island to be tested. Consequently, Appellant respectfully submits that the term "interface" is described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims.

Appellant respectfully submits that the term "snooper" is described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims. It is well accepted that the term snooper is applied to an entity monitors, or snoops, for an output. In the present application, the term snooper is used in a manner consistent with the art. In the present application, a snooper is coupled to an interface, monitors that interface for an output, and provides the output to the checker. Specification, page 12, lines 11-12, Figure 7A and the accompanying discussion. Further, as stated in the Second Declaration, ordinary skill in the art would readily realize that each snooper can be considered to include a physical portion and a logical portion, which is termed the intelligence in the specification. The physical portion of the snooper merely includes interfaces and a mechanism for controlling the interfaces. The intelligence of the snooper is used to control the functions of the snooper. The functions of the snooper are relatively simple and an algorithm to implement such a snooper has been disclosed

on a flow-chart level in Figure 7A. Once coupled to an interface, the snooper merely monitors the interface, waits for an output, and, if detected, provides at least the output to the checker. Although particular outputs are not described, Appellant respectfully submits that particular inputs and outputs depend upon the integrated circuit being tested and the particular simulation being run. Furthermore, the part of the purpose of the snooper is to be reused on multiple integrated circuits. Specification, page 19, lines 4-5. Specifically tying the snooper to a particular integrated circuit or simulation could, therefore, reduce its utility. Consequently, although a detailed algorithm for the snooper is not disclosed, given the functions of the snooper, the use of the term in the art, and the description of the snooper in the specification, one of ordinary skill in the art would understand the recited snooper. Consequently, Appellant respectfully submits that the term "snooper" is described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims.

Appellant respectfully submits that the term "checker" is described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims. As its name implies, a checker primarily checks the output to determine whether the behavior of the island is correct. In particular, as described in the specification, the checker "checks the output against a desired output to determine whether the behavior of island is as expected." Specification, page 12, lines 17-18. Thus, the checker might, for example, simply compare the output to the desired output to determine whether a match has been obtained. The checker recited in the specification also generates the desired output based upon the inputs provided to the island. Specification, page 12, lines 18-20. Further, as stated in the Second Declaration, ordinary skill in the art would

readily realize that each checker can be considered to include a physical portion and a logical portion, which is termed the intelligence in the specification. The physical portion of the checker merely includes interfaces and a mechanism for controlling the interfaces. The intelligence of the checker is used to control the functions of the checker. The functions of the checker are depicted in on a flow-chart level in Figure 7B and described in the accompanying discussion. In particular, the checker receives the input(s), receives the output from the snooper, generates the desired output, checks the output against the desired output and, based on the comparison, may provide a message indicating whether there is an error in the island. See also, specification, page 12, lines 17-20; page 16, lines 10-14; and page 18, lines 1-5. The checker receives such data and provides the messages over its interfaces. Thus, the functions of the checker and the physical portion of the checker which is used in providing the functions of the checker are described in the specification. Appellant respectfully submits that the inputs and output received by the checker, as well as the desired output depend upon the particular island being tested and the particular simulation being run. For example, the value of the desired output generated and, therefore, whether the outcome of the comparison of the desired output may depend upon the simulation being run. Consequently, tying the checker to a particular integrated circuit or simulation could reduce its utility. Thus, although a detailed algorithm for the checker is not disclosed, given the functions of the checker, the use of the term in the art, and the description of the checker in the specification, one of ordinary skill in the art would understand the recited checker. Consequently, Appellant respectfully submits that the term "checker" is described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims.

Appellant respectfully submits that the term "generator" is described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims. A generator generates the inputs that are provided to the island, thereby simulating a device attached to the interface of the island. Specification, page 12, line 20-page 13, line 1. Preferably, the generator also randomizes the inputs to improve testing of the island. Specification, page 13, lines 1-2. Further, as stated in the Second Declaration, ordinary skill in the art would readily realize that each generator can be considered to include a physical portion and a logical portion, which is termed the intelligence in the specification. The physical portion of the generator merely includes interfaces and a mechanism for controlling the interfaces. The intelligence of the generator is used to control the functions of the generator. For example, Figure 7C and the accompanying discussion describe the functions of the generator on the flow-chart level. In particular, the generator receives instructions from the test case, optionally receives outputs from the island, and calculates, or generates, the inputs provided to the island. The recited generator receives instructions from the test case in the form of data and a request that a particular simulation be run on the island. See, for example, specification, page 13, lines 17-19 and page 19, lines 7-10. As indicated in the Second Declaration, the test case thus requests the generator to perform a particular simulation of the island and provides data for the simulation. In addition, as stated in the Second Declaration, one of ordinary skill in the art will readily recognize that in requesting that the generator perform a particular simulation, the test case calls functions provided by, or procedures contained in, the intelligence of the generator. As stated in the Second Declaration, one of ordinary skill in the art will also recognize that the intelligence of the generator helps carry out the desired procedures called by the test case, including providing the

appropriate and preferably randomized inputs to the island in response to a request for service from the test case. The intelligence of the generator also uses the data provided by the test case to generate these inputs. Appellant respectfully submits that the inputs calculated by the generator, the data provided by the test case, and the particular simulation requested depend upon the particular island being tested and the particular simulation being run. Consequently, tying the generator and test case to a particular integrated circuit or simulation could reduce their utility. Thus, although a detailed algorithm for the generator and the specific procedures called or data provided by the test case are not described, given the functions of the generator and the description of the generator in the specification, one of ordinary skill in the art would understand the recited generator, as well as how a test case might control the generator and access particular functions within the generator by providing data and a request for particular simulations. Consequently, Appellant respectfully submits that the term "generator" is described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims.

In addition, as indicated in the Second Declaration, the intelligence of the snooper, checker and generator can be viewed as providing internal data structure (buffering and queuing) and a process for manipulating these data structures in response to service request by other snooper, checker and generator combinations and test case(s) via a set of procedure calls and global signals. The physical and logical parts of each snooper, checker and generator communicate with each other via a set of internal signals. In one embodiment, the logical part operates in simulator's delta-time domain. Communication between the snooper, checker, and generator is also described in Thus, in addition to understanding the individual snooper,

checker, and generator, one of ordinary skill in the art would also understand how these modules function together.

Claims 10 and 17 recite monitoring (or snooping), checking, and generating steps that are analogous to the snooper, checker, and generator recited in claim 1. Consequently, the discussion above applies with full force to the terms monitoring, checking, and generating steps of claims 10 and 17. Accordingly, Appellant respectfully submits that the terms in independent claims 1, 10, and 17 are described in the specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected, to make and/or use the invention, the subject matter of the claims.

Claims 2, 3, 4, 5, 6, 7, 8, and 9 depend upon independent claim 1. Claims 11, 12, 13, 14, 15, and 16 depend upon independent claim 10. Claims 17, 18, 19, 20, 21, 22, and 23 depend on independent claim 17. Consequently, claims 2-9, 11-16, and 18-23 are allowable for the same reasons discussed above with respect to claims 1, 10, and 17.

Accordingly Appellant respectfully requests that the Board reverse the final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 under 35 U.S.C. § 112.

D. Claims 1-23 Are Not Unpatentable Under 35 U.S.C. § 103.

Appellant respectfully submits that the applied rejections of claims 1-23 under 35 U.S.C. § 102(e) as being unpatentable over Hollander in view of Guruswamy are without merit. In particular, the Examiner has completely failed to explain why Hollander in view of Guruswamy teaches or suggests the system, method, and computer-readable medium recited in claims 1, 10, and 17, respectively. Furtherer, the Examiner has failed to explain why Hollander in view of

Guruswamy teaches or suggest the systems, methods, and computer-readable media recited in claims 2-9, 11-16, and 18-23, respectively.

Claims 1, 10, and 17 recite a system, method, and computer-readable medium for providing simulation of an integrated circuit during development of the integrated circuit. The integrated circuit includes one or more interfaces. The system, method and computer-readable medium include a checker that determines a desired output based upon an input to the island and checks the output to determine whether the output is the desired output. Also recited in claims 1, 10 and 17 are a snooper and generator. The snooper is coupled with the interface, monitors the interface, and obtains an output provided by the island during simulation. The generator provides the input to the island during simulation. The generator does so in response to a request from a test case that a particular simulation be performed on the island. The generator also includes the intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator.

Thus, the checker can both generate desired outputs and check the outputs from the island under test against the desired inputs. Using the system, method and computer-readable medium recited in claims 1, 10, and 17, step-wise checking of the behavior of the integrated circuit can be performed. Specification, page 16, lines 13-14. Furthermore, during integration, the generator can be replaced by another island, which provides the inputs to the island, while the snooper and checker can still check the island via the internal interface. Specification, page 13, lines 10-16. In addition, because the snooper, checker and generator can perform the functions recited, the test case(s) need not contain intelligence for controlling specific functions of the snooper, checker and generator. Specification, page 13, lines 7-20. Consequently, the test case(s), many of which may be required for testing of the IC, are simpler to provide. Specification, page 13,

lines 4-5. In addition, the snoopers, checkers, and generators may be reused, thereby conserving resources. Specification, page 19, lines 3-4.

In contrast to the present invention as recited in varying scope in claims 1, 10 and 17, Hollander in view of Guruswamy fails to teach or suggest the use of a checker that both generates the desired inputs and checks the actual inputs against the desired inputs. As described above, the cited portion of Hollander describes synchronizing checking and test generation as part of dynamic checking performed using the method and system described in Hollander. However, Applicant has found no mention in the cited portion of Hollander that the synchronizing could or should include using the checking module to generate the desired outputs based upon the inputs from the test generation module. The cited portions of Hollander merely describe the checking and synchronization performed using the checking module of Hollander. It is quite possible that the checking module receives the desired outputs from the test generation module. Thus, even if the system of Hollander responds to the outputs of the device under test, Applicant can find no indication that it is the checking module, not the test generation module or some other module, that determines the desired outputs. Consequently, Hollander fails to teach or suggest the recited system, method, and computer-readable medium in which the checker both generates the desired inputs and checks the actual inputs against the desired inputs

Guruswamy fails to remedy the defects of Hollander. Although Guruswamy does describe dividing an IC into islands, Appellant can find no mention in the cited portions of Guruswamy of using a checker to not only check the outputs of the island under test, but also to generate the desired outputs based upon the inputs. Thus, if the teachings of Guruswamy are combined with those of Hollander, the combination might use the system of Hollander to check the performance of a circuit laid out in accordance with the teachings of Guruswamy. However, because neither the

cited portions of Hollander nor the cited portions of Guruswamy describe using the checker to both generated the desired outputs based on the inputs and check the outputs against these desired outputs, any combination of Hollander and Guruswamy would also omit this feature. Hollander in view of Guruswamy thus fail to teach or suggest a system, method, or computer-readable medium that includes a checker that generates desired output based upon the inputs to the island and checks the actual outputs against the desired outputs. Accordingly, Appellant respectfully submits that independent claims 1, 10 and 17 are allowable over the cited references.

Claims 2, 3, 4, 5, 6, 7, 8, and 9 depend upon independent claim 1. Claims 11, 12, 13, 14, 15, and 16 depend upon independent claim 10. Claims 17, 18, 19, 20, 21, 22, and 23 depend on independent claim 17. Consequently, claims 2-9, 11-16, and 18-23 are allowable for the same reasons discussed above with respect to claims 1, 10, and 17.

Accordingly Appellant respectfully requests that the Board reverse the final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 under 35 U.S.C. § 103.

E. Summary of Arguments

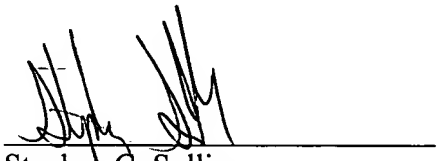
For all the foregoing reasons, it is respectfully submitted that Claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, and 23 (all the claims presently in the application) are patentable for defining subject matter which would not have been obvious under 35 U.S.C. § 103 or and contain only subject matter described in the specification in a manner which comports with the requirements of 35 U.S.C. § 112, first paragraph. Thus, Appellant respectfully requests that the Board reverse the rejection of all the appealed Claims and find each of these Claims allowable.

Note: For convenience of detachment without disturbing the integrity of the remainder of pages of this Appeal Brief, Appellant's "APPENDIX" section is contained on separate sheets following the signatory portion of this Appeal Brief.

This Brief is being submitted in triplicate, and authorization for payment of the required Brief fee is contained in the cover letter for this Brief. Please charge any fee that may be necessary for the continued pendency of this application to Deposit Account No. 50-0563 (IBM Corporation).

Very truly yours,

SAWYER LAW GROUP LLP



September 16, 2003
Date

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IX. APPENDIX

1. A system for providing simulation of an integrated circuit during development of the integrated circuit, the integrated circuit having an island including an interface, the system comprising:

a snooper coupled with the interface for monitoring the interface and obtaining an output provided by the island during simulation;

a checker, coupled with the interface, for checking the output to determine whether the output is a desired output;

a generator coupled with the island for providing an input to the island during simulation; and

at least one test case coupled with the generator for directing the generator;

wherein the checker further determines the desired output based upon the input; and

wherein the generator further includes intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator, the request requesting that the generator perform a particular simulation on the island.

2. The system of claim 1 wherein the checker is coupled with the snooper and wherein the checker receives the output from the snooper.

3. The system of claim 1 wherein the snooper may be reused when the island is integrated with a second island.

4. The system of claim 1 wherein the checker may be reused when the island is integrated with a second island.

5. The system of claim 1 wherein the generator may be reused when the island is integrated with a second island.

6. The system of claim 1 wherein the generator receives the output and provides the input based on the output.

7. The system of claim 1 wherein the generator and the snooper are coupled with the interface, wherein the checker is coupled with the interface through the snooper and wherein only the snooper and the checker are reused when a second island is integrated with the island at the interface.

8. The system of claim 1 wherein the at least one test case further provides data and instructions to the generator.

9. The system of claim 1 wherein the interface is an internal interface.

10. A method for providing simulation of an integrated circuit during development of the integrated circuit, the integrated circuit having an island including an interface, the method comprising the steps of:

(a) monitoring the interface to obtain an output provided by the island during simulation;

(b) checking the output to determine whether the output is a desired output, the checking step (b) further including the step of

(b1) determining the desired output based upon an input;

(c) providing the input to the island during simulation; and

(d) directing the providing of the input using at least one test case;

wherein the input is provided to the island using a generator including intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator, the request requesting that the generator perform a particular simulation on the island.

11. The method of claim 10 wherein step (a) further includes the step of:

(a1) snooping the interface to obtain the output provided by the island during simulation using a snooper, the snooper capable of being reused when the island is integrated with a second island.

12. The method of claim 10 wherein step (b) further includes the step of:

(b1) checking the output using a checker to determine whether the output is the desired output, the checker capable of being reused when the island is integrated with a second island.

13. The method of claim 10 wherein step (c) further includes the step of:

(c1) providing the input to the island during simulation using a generator, the generator capable of being reused when the island is integrated with a second island.

14. The method of claim 10 wherein step (c) further includes the step of:

(c1) providing an input to the island during simulation using a generator, the generator receiving the output and providing the input based on the output.

15. The method of claim 14 wherein the directing step (d) further includes the step of:

(d1) providing data and instructions from the at least one test case to the generator.

16. The method of claim 10 wherein the interface is an internal interface.

17. A computer-readable medium having a program for providing simulation of an integrated circuit during development of the integrated circuit, the integrated circuit having an island including an interface, the program comprising instructions for:

(a) monitoring the interface to obtain an output provided by the island during simulation;

(b) checking the output to determine whether the output is a desired output, the checking step (b) further including the step of

(b1) determining the desired output based upon an input;

(c) providing the input to the island during simulation; and

(d) directing the providing of the input using at least one test case;

wherein the input is provided to the island using a generator including intelligence to provide the input to the island based only upon data and a request provided by the at least one test case to the generator, the request requesting that the generator perform a particular simulation on the island.

18. The computer-readable medium of claim 17 wherein the instruction for snooping (a) further includes the instructions for:

(a1) snooping the interface to obtain the output provided by the island during simulation using a snooper, the snooper capable of being reused when the island is integrated with a second island.

19. The computer-readable medium of claim 17 wherein the instruction for checking (b) further includes instructions for:

(b1) checking the output using a checker to determine whether the output is the desired output, the checker capable of being reused when the island is integrated with a second island.

20. The computer-readable medium of claim 17 wherein the input providing step (c) further includes instructions for:

(c1) providing the input to the island during simulation using a generator, the generator capable of being reused when the island is integrated with a second island.

21. The computer-readable medium of claim 17 wherein the input providing step (c) further includes instructions for:

(c1) providing an input to the island during simulation using a generator, the generator receiving the output and providing the input based on the output.

22. The computer-readable medium of claim 17 wherein the directing instructions (d) further includes the instructions for:

(d1) providing data and instructions from the at least one test case to the generator.

23. The computer-readable medium of claim 17 wherein the interface is an internal interface.